CLAIMS

We claim:

1. A process, in integrated circuit production, for filling a gap having an opening of initial width in the surface of a substrate, comprising:

first depositing a film in said gap using an HDP CVD process having an etch/dep ratio less than one;

stopping said first depositing before said opening closes;

chemically etching said film in said gap with a hydrogen-based plasma;

stopping said etching before corners of elements forming said gap are exposed; and

later depositing a film in said gap.

2. The process of Claim 1, further comprising applying a high frequency (HF) power to bias said substrate.

3. The process of Claim 2, wherein said etching is without argon.

4. The process of Claim 1, wherein said substrate is unbiased.

5. The process of Claim 1, wherein said first depositing is stopped before said opening closes.

6. The process of Claim 1, wherein said depositing is performed with a gas mixture comprising oxygen and silane.

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7. The process of Claim 6, wherein said gas mixture further comprises an inert gas.

8. The process of Claim 1, further comprising repeating one or more cycles of said first depositing and said etching until said gap is filled without leaving a void in said gap.

9. The process of Claim 1, wherein said film is undoped silica glass.

10. The process of Claim 1, wherein said film is doped silica glass.

11. The process of Claim 1, wherein said substrate is attached to and heated or cooled by a thermally controllable electrostatic chuck.

12. The process of Claim 11, wherein said electrostatic chuck is resistively heated.

13. The process of Claim 11, wherein said substrate attached to said electrostatic chuck is cooled with backside flow of helium.

14. The process of Claim 1, wherein said chemically etching is in accordance with the reaction $SiO_2 + 2H_2 \rightarrow SiH_4 + O_2$.

15. The process of Claim 1, wherein energy for said chemically etching is from a plasma from the HDP CVD process.

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16. The process of Claim 1, wherein the etch rate for said chemically etching is of the order of 100 Å/min.

17. The process of Claim 1, wherein the rate of said chemically etching increases with low frequency power is increased.

18. The process of Claim 1, wherein said etching is performed by a non-fully directional etching process.

19. The process of Claim 1, wherein said etching is performed in situ.

20. The process of Claim 1, wherein said first depositing and said etching are performed in a single process chamber.

21. A process, in integrated circuit production, for depositing an oxide film to fill a gap having an opening of initial width in the surface of a substrate of a less than or equal to about 0.13 microns and a depth, wherein the ratio of said depth to said initial width defines a high aspect ratio of about 3.5:1 or greater, said process comprising:

first depositing an oxide film in said gap using an HDP CVD process having an etch/dep ratio less than one;

stopping said first depositing before said opening is closed;

chemically etching, in situ, said oxide film in said gap with an HDP etching process with a hydrogen-based plasma;

stopping said etching before corners of elements forming said gap are exposed; and

later depositing an oxide film in said gap.

22. The process of Claim 21, further comprising applying a high frequency (HF) power to bias said substrate.

23. The process of Claim 22, wherein said etching is without argon.

24. The process of Claim 21, wherein said substrate is unbiased.

25. The process of Claim 21, wherein said etching is performed with a non-fully directional etch process.

26. The process of Claim 21, wherein said first depositing and said etching are performed in a single process chamber.

27. The process of Claim 21, wherein said chemically etching is in accordance with the reaction $SiO_2 + 2H_2 \rightarrow SiH_4 + O_2$.

28. The process of Claim 21, wherein energy for said chemically etching is from a plasma from the HDP CVD process.

29. The process of Claim 21, wherein the etch rate for said chemically etching is of the order of 100 Å/min.

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30. The process of Claim 21, wherein the rate of said chemically etching increases with low frequency power is increased.

31. A process for etching deposited material in an HDP CVD process, comprising:

introducing hydrogen into a plasma chamber;

reacting the hydrogen with the deposited material to chemically etch the deposited material.

32. The process of Claim 31, wherein said deposited material is a silicon oxide.

33. The process of Claim 32, wherein said reacting produces silane and oxygen.

34. The process of Claim 31, wherein the energy for said reacting is provided by the plasma.

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